

#3

1 / 14

FIG. 1

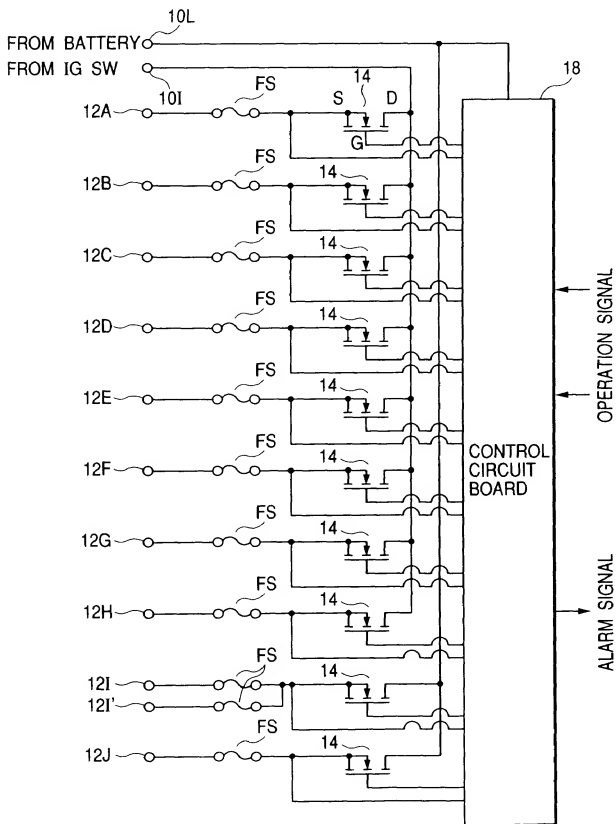


FIG. 2

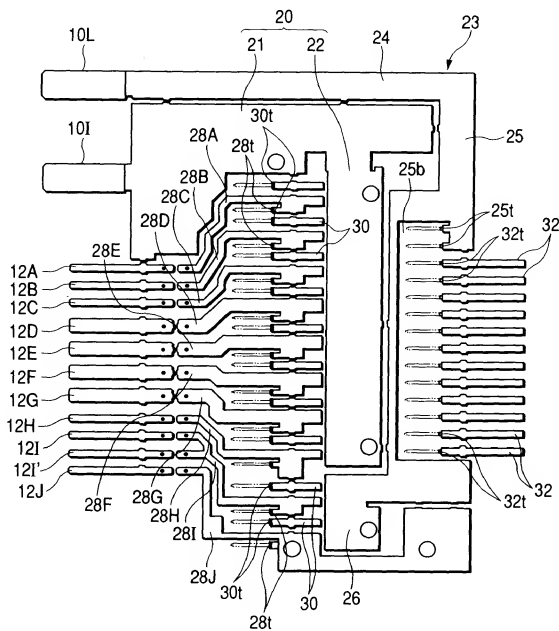


FIG. 3

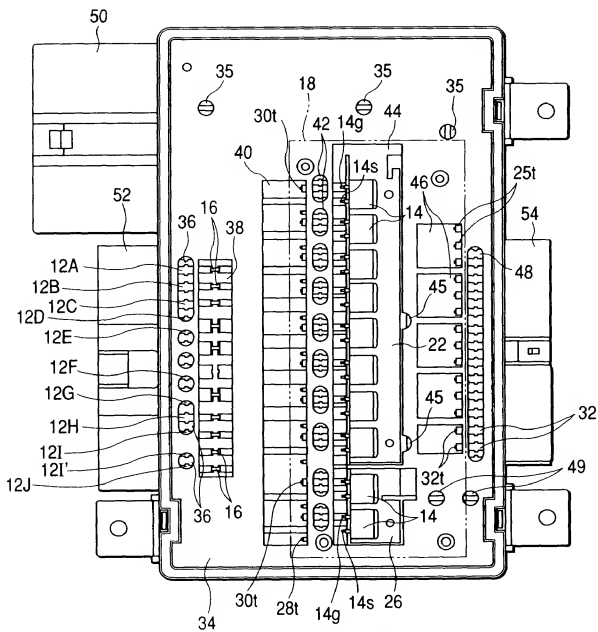


FIG. 4A

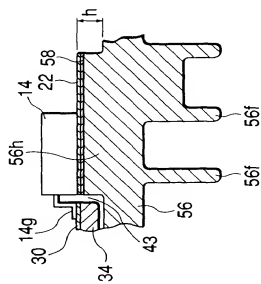
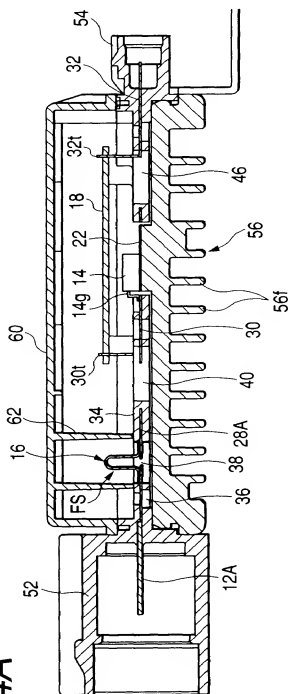


FIG. 4B

**FIG. 5B**

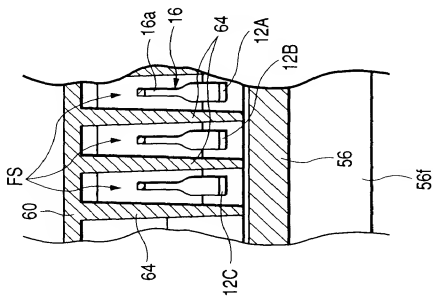


FIG. 6

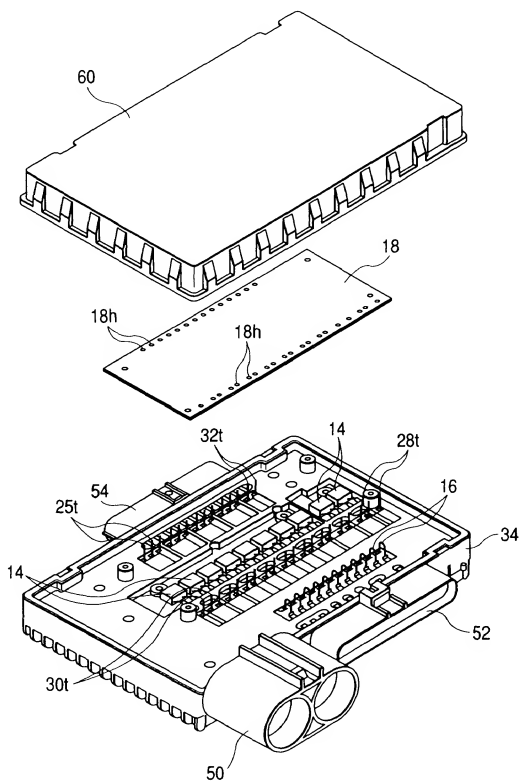
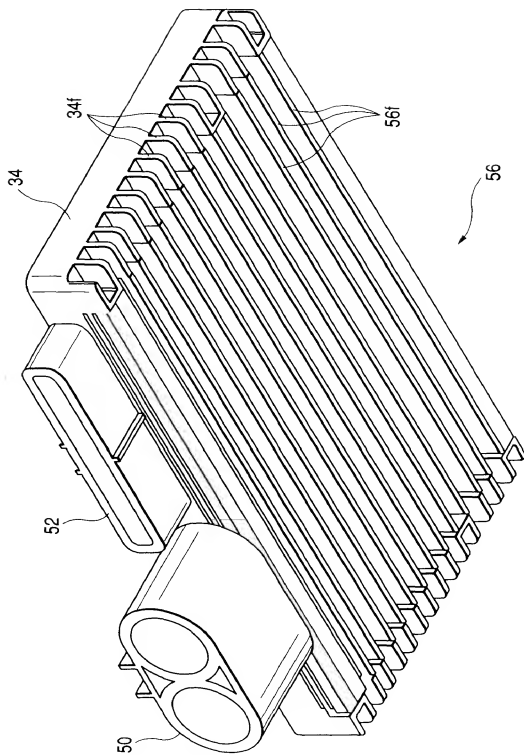


FIG. 7



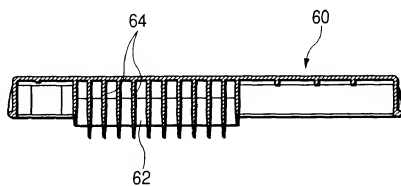
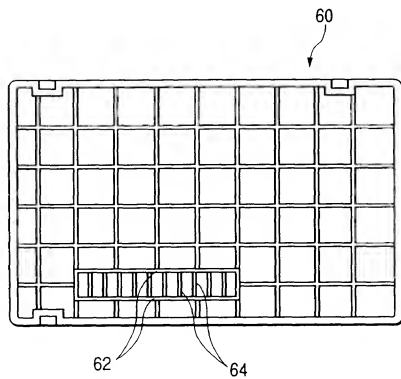
*FIG. 8A**FIG. 8B*



FIG. 9

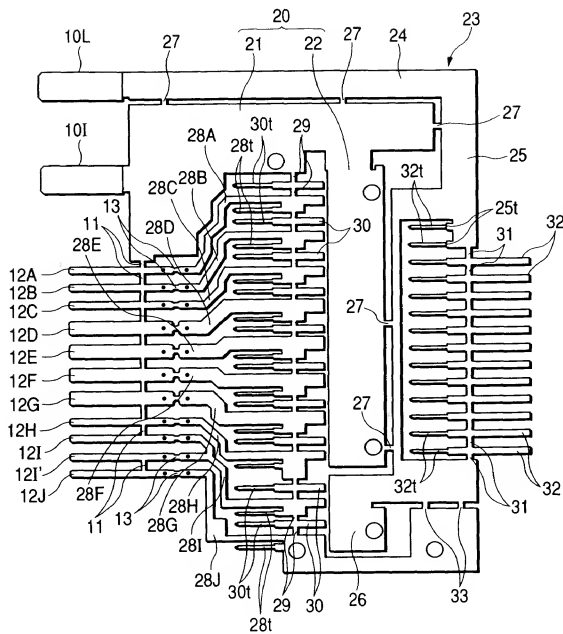


FIG. 10

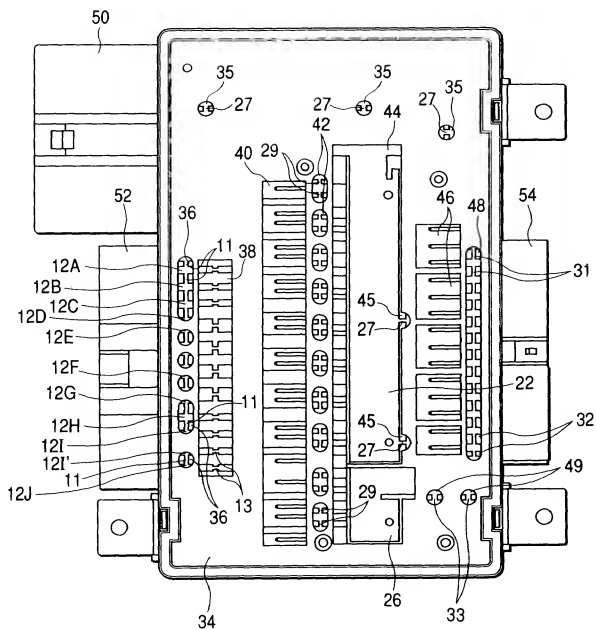
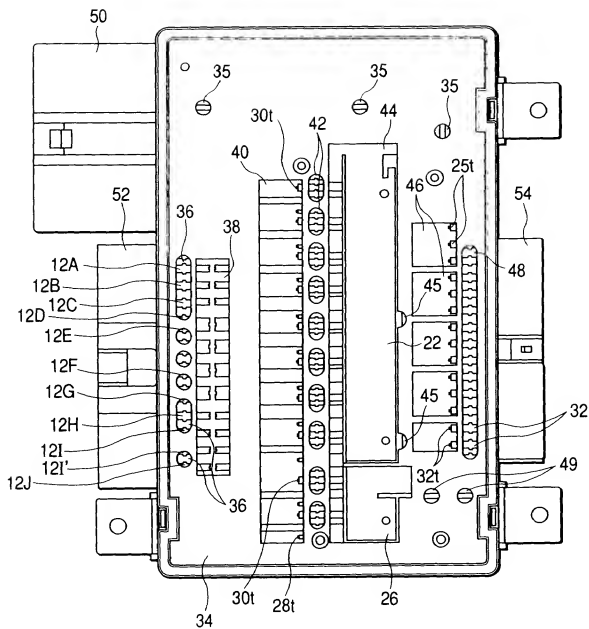


FIG. 11



The diagram illustrates a complex semiconductor device layout. Key features include:

- Input/Output Pads:** Labeled 10L and 10I on the left; 20, 21, 23, and 24 along the top.
- Internal Structures:** 21a, 22, 22a, 25, 25t, 25b, 26a, 28A through 28J, 30, 30t, 32, and 32t.
- Interconnects:** A series of horizontal lines labeled 12A through 12J connecting different sections of the chip.

FIG. 13

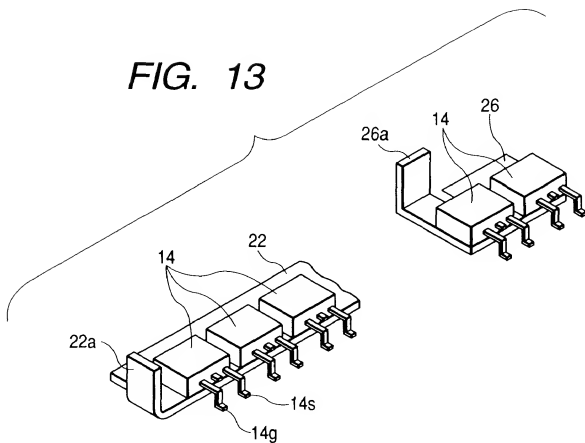


FIG. 14

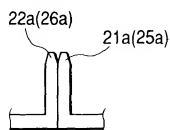


FIG. 15

